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10/609,158	06/27/2003	Nathan Laredo	TRAN-P206	7870

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,158	LAREDO ET AL.	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

2. This action is in response to the Amendment on 3/23/09. Applicant's arguments have been fully considered but they are considered moot in view of the new grounds of rejections.

Claim Objections

3. Claims 5, 15, and 25 are objected to because of the following informalities:

In claim 5, line 2, the limitation "causes the monitor single step" should be amended to – causes the monitor to single step – in order to correct the grammatical error. Claims 15 and 25 are objected for the same reasons.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine et al. (hereinafter Devine) (US 6,397,242 B1) in view of Dornan et al. (hereinafter Dornan) (US 7,089,539 B2), and further in view of Waldspurger et al. (hereinafter Waldspurger) (US 7,260,820 B1).

5. As to claim 1, Devine teaches a method for supporting input/output for a virtual machine (see Fig. 1-2), comprising:

executing virtual machine application instructions (col. 2, lines 27-35, col. 9, lines 11-12, etc.);

receiving an I/O access from the virtual machine application (col. 2, lines 21-36, col. 13, lines 20-36, Fig. 1-2);

upon receiving the I/O access, generate an exception (col. 7, lines 6-13, col. 8, lines 40-43);

performing the I/O access by using a host operating system (col. 11, lines 34-40, col. 12, line 50);

updating state data for the virtual machine application in accordance with the I/O access (col. 5, lines 60-67 through col. 6, lines 1-6); and

resuming execution of the virtual machine application from the exception (Resume 242, Fig. 2, col. 21, lines 56-60).

6. Devine is explicitly silent in the use of micro architecture code of a processor architecture code. However, Dornan discloses a computer system with micro architecture code of a processor code to feed pipelines of the processor architecture hardware, including a hardware instruction interpreter to execute the VM application instructions (Abstract, col. 1, lines 47-67, Fig. 11, item 126). Devine and Dornan are analogous art because they are both in the same field of endeavor of executing a virtual machine. One of ordinary skill in the art would have known to modify Devine's virtual machine system such that it would include the processing hardware device for

executing virtual machine instructions that include the use of micro architecture code, as taught in Dornan. The suggestion/motivation for doing so would have been to provide the predicted result of being able to use the hardware interpreter to focus on performance critical mappings to produce a significant performance gain with relatively little additional hardware overhead (col. 2, lines 2-6, Abstract). Devine and Dornan are silent in teaching a monitor that receives the I/O access, generates exceptions, and updates state data. However, Waldspurger teaches I/O operations between virtual machine and a device external to the VM are monitored by a virtual machine monitor (VMM) that receives the I/O access, generates exceptions, and updates state data (Fig. 1, items 300, 400, 430, 470, Abstract, col. 2, lines 45-57, col. 5, lines 35-67, col. 6, lines 1-10). Devine, Dornan and Waldspurger are all analogous art because they are all in the same field of endeavor of executing a virtual machine. One of ordinary skill in the art would have known to modify Devine in view of Dornan's virtual machine system such that it would include the features of a monitor that receives the I/O access, generates exceptions, and updates state data, as taught in Waldspurger's virtual machine system. The suggestion/motivation for doing so would have been to provide the predicted result of improving the control and security of the system (col. 1k lines 6-11 and 40-67, col. 2, lines 45-60). Therefore, it would have been obvious to one of ordinary skill in the art to combine Devine, Dornan, and Waldspurger to obtain the invention of claim 1.

7. As to claim 2, Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches wherein the micro architecture code comprises an instruction interpreter is further configured to function with an instruction translator to translate target instructions into host instructions to execute the

virtual machine application instructions. Devine teaches that virtual machine processing with a VLIW architecture (col. 2, lines 30-36).

8. As to claim 3, Devine (Fig. 2, 230) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches wherein the micro architecture code comprises an instruction translator to execute the virtual machine application instructions.

9. As to claim 4, Devine teaches further comprising: executing the monitor to implement the I/O access from the virtual machine application, wherein the monitor is configured to handle the exception caused by the I/O access (virtual machine monitor, see Abstract, col. 5, lines 13-30).

10. As to claim 5, Devine teaches further comprising:

entering the single step mode, wherein the single step mode causes the monitor single step through the virtual machine application instructions to handle the exception (col. 11, lines 34-48, col. 12, lines 49-52).

11. As to claim 6, Devine (col. 24, lines 63-67) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches further comprising: using the monitor to maintain at least one virtual device to implement the I/O access from the virtual machine application.

12. As to claim 7, Devine teaches further comprising:

using the host operating system to access a real device in response to an access to the virtual device (Fig. 7, 700, 720, 750, 710, 100, col. 24, lines 60-67, etc.); and

updating the state data for the virtual machine application in accordance with I/O data retrieved from the real device (col. 5, lines 60-67 through col. 6, lines 1-6).

13. As to claim 8, Devine (see Fig. 1, col. 2, lines 27-35, col. 9, lines 11-12) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teach wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions.

14. As to claim 9, Devine (col. 2, line 32) teaches wherein the target instructions comprises x86 instructions and the host instructions are VLIW instructions.

15. As to claim 10, Devine teaches wherein the virtual machine comprises an x86 compatible virtual machine (col. 9, lines 7-11).

16. As to claim 11, it is rejected for the same reasons as stated in the rejection of claim 1. In addition, Devine teaches a system for supporting input/output for a virtual machine (Fig. 1-2), comprising: a processor architecture including micro architecture code configured to execute, natively on a CPU hardware unit of the processor architecture (col. 2, lines 27-35, col. 9, lines 11-12); and a memory coupled to the processor architecture, the memory storing virtual machine application instructions, wherein the application instructions are executed using the micro

architecture code, the micro architecture code causing the processor architecture to implement a method comprising (col. 13, lines 20-36).

17. As to claims 12-21, they are rejected for the same reasons as stated in the rejections of claims 2-11.

18. As to claims 22-30, they are rejected for the same reasons as stated in the rejections of claims 2-10.

Response to Arguments

19. During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

20. Applicant's arguments have been fully considered and not found to be persuasive. Applicant attacks the reference of Devine individually. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642

F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In response to the newly amended claims, new grounds of rejections have been presented based on the combination of the references of Devine, Dornan and Waldspurger.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Ogi (US 5,361,375)** discloses a virtual computer system having input/output interrupt control of virtual machines (see Abstract).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194

/Kenneth Tang/
Examiner, Art Unit 2195